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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/527,560	03/11/2005	Gerardus T.M. Hubert	NL02 0922 US	7448

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EXAMINER	
SANDERS, STEPHEN	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/527,560	HUBERT, GERARDUS T.M.	
	Examiner	Art Unit	
	STEPHEN SANDERS	2139	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *Mar. 11, 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is in response to Application/Control Number: 10/527,560 filed on March 11, 2005 in which claims 1-35 are presented for examination.

Status of Claims:

Claims 1-35 are pending, of which claims 1, 20, 34, and 35 are in independent form.

Claims 1-35 are rejected under 35 U.S.C. 102(e).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Leydier U.S. Patent Number 6,848,619; Date of Patent: Feb. 1, 2005; Filing Date: Jul. 1, 2002; hereinafter Leydier.

As to claim 1, the following is taught: "A data processing device including:

a processor (Leydier: Abstract; column 2, lines 17-27; column 9, lines 54-57);

a charge storage device coupled to the processor (Leydier: Abstract; column 5, lines 41-50; Figure 9; column 8, lines 31-36); and

a current source for supplying the processor with operating current, and adapted to vary its output current independently of the instantaneous power demand of the processor (Leydier: column 3, lines 17-30; column 10, lines 1-3)."

As to claim 2, the following is taught: "The device of claim 1 in which the charge storage device comprises a capacitor in series with the current source, and across which the processor is connected in parallel (Leydier: column 2, lines 50-53; column 4, lines 65-67)."

As to claim 3, the following is taught: "The device of claim 1 in which the current source is adapted to periodically or aperiodically switch between two different current levels (Leydier: column 2, lines 38-60; column 8, lines 54-67).

As to claim 4, the following is taught: "The device of claim 1 in which the current source is adapted to periodically or aperiodically switch between multiple current levels (Leydier: column 2, lines 38-60; column 8, lines 54-67; column 9, lines 17-27).

As to claim 5, the following is taught: "The device of claim 3 in which the interval between switching current levels is determined by an average power demand of the processor (Leydier: column 6, line 56 to column 7, line 13; column 8, lines 7-17)."

As to claim 6, the following is taught: "The device of claim 1 in which the current source comprises:

a first current source adapted to provide substantially constant current at at least two different current levels, the first current source switching between current levels on a periodic or aperiodic basis (Leydier: column 2, lines 38-53; column 4, lines 41-47; column 5, lines 41-50);

and a second current source adapted to provide a noise current that varies on a random or pseudo-random basis (Leydier: column 8, lines 54-67; column 10, lines 19-21)."

As to claim 7, the following is taught: "The device of claim 1 further including control means adapted to maintain the supply voltage to the processor between an upper voltage limit and a lower voltage limit (Leydier: Abstract; column 2, lines 27-60; column 4, lines 47-57)."

As to claim 8, the following is taught: "The device of claim 1 further including a zener diode adapted to maintain the supply voltage to the processor below an upper voltage limit (Leydier: column 5, lines 11-28; column 5, line 65 to column 6, line 17)."

As to claim 9, the following is taught: "The device of claim 7 in which the control means includes current switching means for switching the current source between a first, higher current level and a second, lower current level, the current switching being

triggered by the supply voltage to the processor respectively reaching the lower voltage limit and the upper voltage limit (Leydier: column 8, lines 50-63)."

As to claim 10, the following is taught: "The device of claim 9 further including a timer for determining a time period taken for the processor supply voltage to reach a lower voltage limit from an upper voltage limit, or vice versa (Leydier: column 2, lines 28-60; column 4, lines 20-25)."

As to claim 11, the following is taught: "The device of claim 10 further including current setting means for varying the first current level and/or the second current level of the current source if the timer determines that the time period falls outside predetermined limits (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 12, the following is taught: "The device of claim 11 in which the current setting means raises the first current level if the timer determines that the time period for reaching the lower voltage limit falls below a first predetermined threshold (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 13, the following is taught: "The device of claim 11 in which the current setting means reduces the first current level if the timer determines that the time

period for reaching the lower voltage limit exceeds a second predetermined threshold (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 14, the following is taught: "The device of claim 11 in which the current setting means reduces the second current level if the timer determines that the time period for reaching the upper voltage limit falls below a first predetermined threshold (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 15, the following is taught: "The device of claim 11 in which the current setting means raises the second current level if the timer determines that the time period for reaching the upper voltage limit exceeds a second predetermined threshold (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 16, the following is taught: "The device of claim 9 in which the control means includes means for temporarily inhibiting the current switching means if the supply voltage to the processor fails to move towards the desired upper or lower voltage limit (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 17, the following is taught: "The device of claim 1 in which the processor has an internal clock, the frequency of which is dependent upon the supply voltage to the processor (Leydier: column 6, lines 19-25; Figure 8)."

As to claim 18, the following is taught: "The device of claim 1 in which the processor is a cryptographic processor (Leydier: Abstract; column 1, lines 31-36; column 4, lines 31-35)."

As to claim 19, the following is taught: "The device of claim 1 incorporated into a smart card (Leydier: Abstract; column 1, lines 21-30; column 2, lines 16-32)."

As to claim 20, the following is taught: "A method of operating a data processing device, comprising the steps of:

drawing current from an external supply (Leydier: Abstract; column 5, lines 41-50; Figure 9; column 8, lines 31-36);

cyclically apportioning drawn current between a charge storage device and a processor within the data processing device such that the drawn current varies independently of the instantaneous power demand of the processor (Leydier: column 3, lines 17-30; column 10, lines 1-3)."

As to claim 21, the following is taught: "The method of claim 20 further including the step of using the drawn current to generate a current flow to the processor and the

charge storage device, that is periodically or aperiodically switched between two different current levels (Leydier: column 2, lines 38-60; column 8, lines 54-67)."

As to claim 22, the following is taught: "The method of claim 20 further including the step of using the drawn current to generate a current flow to the processor and the charge storage device, that is periodically or aperiodically switched between multiple different current levels (Leydier: column 2, lines 38-60; column 8, lines 54-67; column 9, lines 17-27)."

As to claim 23, the following is taught: "The method of claim 21 further including the step of determining the interval between switching according to an average power demand of the processor (Leydier: column 6, line 56 to column 7, line 13; column 8, lines 7-17)."

As to claim 24, the following is taught: "The method of claim 20 further including the steps of:

using a first current source to deliver substantially constant current at at least two different current levels, switching the first current source between current levels on a periodic or aperiodic basis (Leydier: column 2, lines 38-53; column 4, lines 41-47; column 5, lines 41-50);

using a second current source to provide a superposed current that varies on a random or pseudo-random basis and

delivering the combined current of the first and second current sources to the processor and the charge storage device (Leydier: column 8, lines 54-67; column 10, lines 19-21)."

As to claim 25, the following is taught: "The method of any one of claims 20 to 24 further including the step of maintaining a supply voltage to the processor between an upper voltage limit and a lower voltage limit (Leydier: column 5, lines 11-28; column 5, line 65 to column 6, line 17)."

As to claim 26, the following is taught: "The method of claim 25 further including the step of switching a current source between a first, higher current level and a second, lower current level, when the supply voltage to the processor respectively reaches the lower voltage limit and the upper voltage limit (Leydier: column 8, lines 50-63)."

As to claim 27, the following is taught: "The method of claim 26 further including the steps of: determining a time period taken for the processor supply voltage to reach a lower voltage limit from an upper voltage limit, or vice versa, and varying the first current level and/or the second current level of the current source if the time period falls outside predetermined limits (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 28, the following is taught: "The method of claim 27 further including the step of raising the first current level if the time period for reaching the lower voltage limit falls below a first predetermined threshold (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 29, the following is taught: "The method of claim 27 or claim 28 further including the step of reducing the first current level if the time period for reaching the lower voltage limit exceeds a second predetermined threshold (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 30, the following is taught: "The method of claim 27 further including the step of reducing the second current level if the time period for reaching the upper voltage limit falls below a first predetermined threshold (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 31, the following is taught: "The method of claim 27 further including the step of raising the second current level if the time period for reaching the upper voltage limit exceeds a second predetermined threshold (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 32, the following is taught: "The method of claim 26 further including the step of temporarily inhibiting the current switching if the supply voltage to the

processor fails to move towards the desired upper or lower voltage limit (Leydier: column 2, lines 30-53; column 4, lines 13-25; column 4, lines 36-58; column 9, lines 45-52)."

As to claim 33, the following is taught: "The method of claim 20 further including the step of controlling the frequency of operation of the processor as a function of the supply voltage to the processor (Leydier: column 2, lines 38-44)."

As to claim 34, the following is taught: "A data processing device substantially as described herein with reference to the accompanying drawings (Leydier: column 3, lines 36-52)."

As to claim 35, the following is taught: "A method of operating a data processing device substantially as described herein with reference to the accompanying drawings (Leydier: column 3, lines 36-52)."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN SANDERS whose telephone number is (571)270-5308. The examiner can normally be reached on M - F; 7:30a.m. - 5:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kristine L. Kincaid can be reached on 571-272-4063. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen Sanders/
Examiner, Art Unit 2139

/Kristine Kincaid/
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